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Low Voltage Differential Signaling (LVDS), Part 2

LVDS applications, testing, and performance evaluation expand.

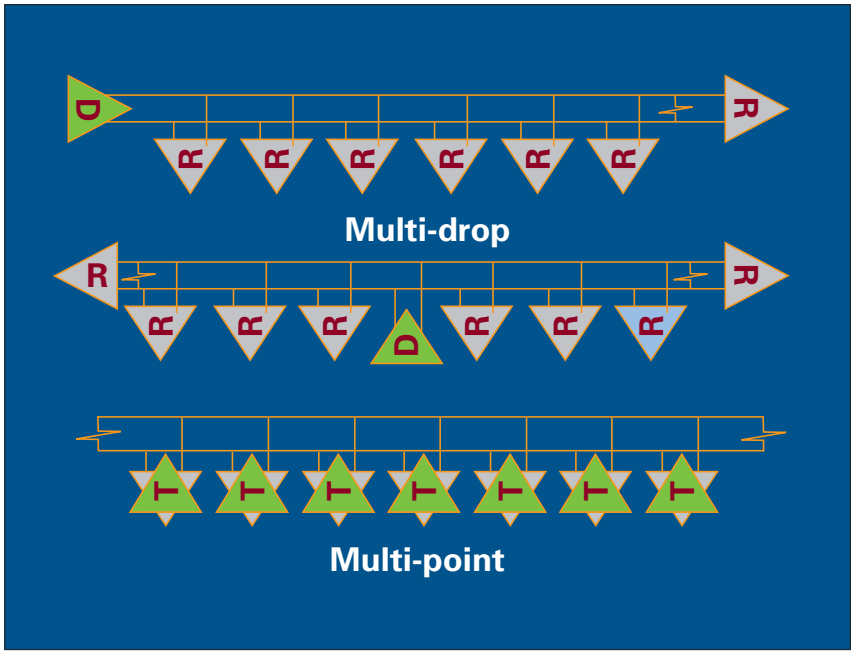


Figure 1. Multidrop and multipoint bus topologies useful in BLVDS applications

The need for high-speed data transmission is exploding as the world becomes ever more interconnected. Data transfers of all types are requiring higher and higher bandwidth as advances are made in fields such as communications, digital video, and color graphics. This need for speed is further fueled by the Internet's infiltration into so many aspects of business, academic, and personal life.

LVDS is a generic interface standard for high-speed data transmission. It uses high-speed analog circuit techniques to provide multi-gigabit data transfers on copper interconnects. Its proven speed, low power, noise control, and cost advantages are popular in point-to-point applications for telecommunications, data communication, and displays.

"Plain" LVDS was described in Part 1 of this article in the previous issue of *Insight* (Volume 5, Issue 2). Part 2 describes variations of LVDS that expand its range of applications, and also covers testing and performance evaluation of high-speed LVDS chips.

Bus LVDS

A review of bus topology helps in understanding the development of Bus LVDS (BLVDS), the first offspring of LVDS. The top two buses in **Figure 1** show multidrop configurations. The top configuration is unidirectional because there is a single driver at one end of the bus. This simple multidrop bus requires only a single termination that is on the opposite end of the bus from the driver, to stop reflections of the driven signal. Each of the attached receivers reduces the loaded bus impedance. The loading amount depends on the connector, vias, packaging, and receiver input capacitance. If these factors are well designed to keep the loading small, plain LVDS can drive this configuration.

The second multidrop bus differs from the first because it is driven from the center rather than the end of the bus. This configuration is useful

for reducing flight-time variations from the driver to all receivers. However, it requires a termination resistor at each end of the bus to prevent reflections. Furthermore, the larger the capacitive loads and the less space between them, the lower the bus's loaded impedance. Because the termination resistors must match this lower impedance to stop reflections, they can be as low as 54Ω in a heavily loaded bus. The two termination resistors are seen in parallel by the driver, so the driver must source as much as three times the current of point-to-point LVDS to drive this bus to a given differential voltage level as it would for the unidirectional bus.

The third bus is a multipoint, bidirectional bus because it has multiple drivers and receivers (transceivers). This is the most difficult bus to design for high performance because of the variable driver positions, which cause various reflections that depend on where the signal originates in the bus. It also must be terminated on both ends to prevent reflections.

The Complexities of Signal Integrity

Signal integrity in a heavily loaded backplane is a very complicated problem due to the many impedance discontinuities inherent in the backplane environment. The worst-case situation in bus signaling occurs when a card in the middle of the bus drives a signal into the backplane and the card in the adjacent slot looks to receive the signal. The edge rate from the driving card is very fast as the signal leaves it and travels down the backplane. The adjacent cards see the fast edge propagate into the signal stub. This fast edge rate causes reflections on the stub that can glitch through the receiver threshold region. (The most important factor for high-speed performance in all bus topologies is keeping each receiver's non-terminated stub very short, minimizing reflections from that stub.)

BLVDS uses the same basic schematic as LVDS, but extends LVDS's point-to-point and simple multidrop applications to true multipoint busing functionality. It does this by boosting the drive current to 10 mA to drive double terminations on heavily loaded buses, and by providing driver output impedance that matches the line impedance to reduce reflections from driver outputs.

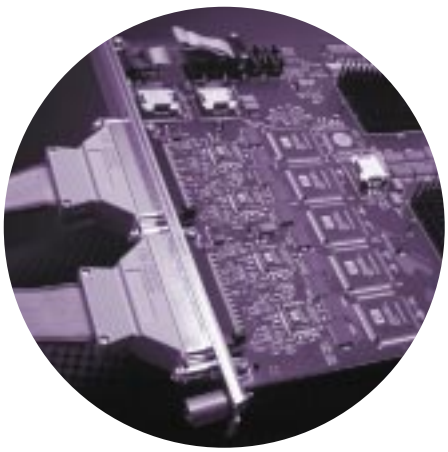
One of the essential features required in a multidrop bus is the ability to insert cards into the bus without powering it down. The optimal hot-insertion capability is to insert cards without stopping or disturbing the data traffic on the bus. BLVDS supports this optimal hot-insertion capability, as the signal glitch caused by inserting the capacitive load of the plug-in card occurs equally on each of the differential lines that have a low impedance connection between them. Therefore there is no change to the differential signal.

Serializer/Deserializer Example

An application example of Bus LVDS technology is the serializer/deserializer chipset. The transmitter serializes a 10-bit parallel LVTTL interface into a single BLVDS data channel, and also embeds the clock in the serial stream. The BLVDS receiver recovers the clock and data to deserialize them back into the 10-bit parallel interface.

This chipset distributes data over a serial channel in multidrop distribution systems. One serializer can drive many deserializers in either of the multidrop configurations shown in **Figure 1**. Multipoint application is also possible with certain limitations due to PLL lock time. The limitations arise when a new driver begins to drive the bus and all the receivers must lock to that driver's clock signal. In addition, the chipset works in point-to-point applications. The chipset supports TTL clock rates from 16 to 66 MHz. For example, the chipset transfers a 660-Mb/s payload over a 10-meter cable when the 10-bit interface operates with a 66-MHz clock.

The chipset's waveform has a 10-bit payload surrounded by two embedded clock bits. The actual serial bit rate with a 40-MHz clock is 480 Mb/s, but the throughput is 400 Mb/s. The receiver uses the embedded clock edges to lock onto the inbound serial stream and to align the data at the parallel output. It provides greater system benefits than other LVDS parts by eliminating the cost of a cable or PCB differential pair for the clock signal.



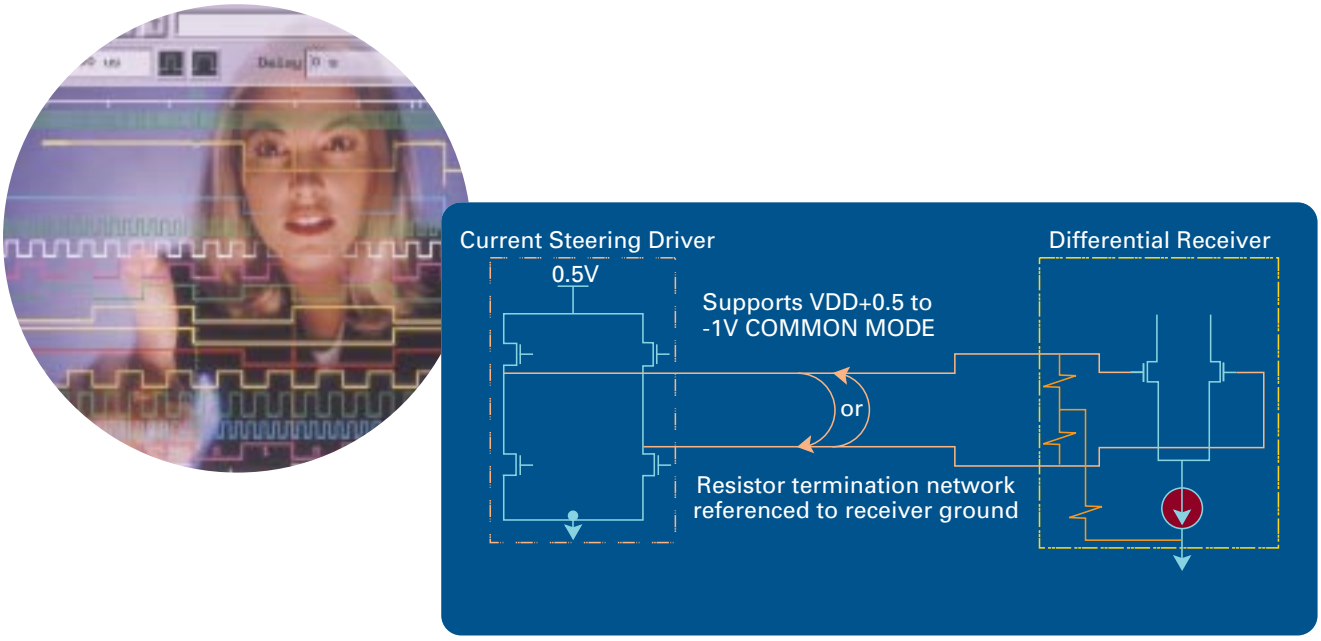


Figure 2. The simplified GLVDS schematic shows its similarity to both LVDS and BLVDS

LVDS in Low-Power Applications

LVDS is also being adapted for very low-power applications, such as a remote base station depending on wind- or sun-generated power. This is Ground-referenced LVDS (GLVDS), which is a proposed standard interface. The JEDEC JC-16 committee for low-voltage interface standards is considering the standard. The proposed standard has transmitter output voltages between 0 V and 0.5 V, and receiver input sensitivity of at least 100 mV. The very low transmitter output voltage provides for low power consumption by the interface. This lower power consumption is an advantage this technology brings to the LVDS family of standards.

The simplified GLVDS schematic shown in **Figure 2** is very similar to both LVDS and BLVDS. One of the few differences is the circuit from the middle of the receiver termination to the receiver's ground. The GLVDS name refers to this ground reference for the receiver termination. GLVDS requires termination to be on-chip rather than an off-chip option, as is the case with LVDS and BLVDS.

Another important feature of this technology is the ability for chips with far different power supplies—from 5 V down to 0.5 V—to communicate with each other. This is possible because all of these power supplies use ground as a common reference. That common ground is the common voltage level where GLVDS signals are working.

The GLVDS standard does not specify any transmitter drive current. The intention is to leave that open to the individual applications that use the interface technology. This would allow the driver to provide a small current (for example, 1.5 mA to 3 mA) for chip-to-chip applications that have short interconnects. For applications that need to drive long cable lengths, the driver would have to supply a larger current output (8 mA to 15 mA).

Test and Evaluation Considerations

There are many considerations with testing and evaluating high-performance LVDS devices. For example, the test equipment needs the two clock rates that result from serializing the parallel data into high-speed signals. The test system must be able to generate and analyze the data at both clock frequencies. Testing the receiver of the Open LVDS Display Interface (OpenLDI) chipset can demonstrate some performance issues.

Figure 3 shows a block diagram of the setup for the OpenLDI DUT interface board. The Agilent 81200 data generator/analyzer is a complete test system capable of 1.32-Gb/s testing (although the system works at a frequency of up to 2.67 Gb/s). The data generator/analyzer achieves 1.32 Gb/s by multiplexing two of the 660-Mb/s

channels into one generator or analyzer channel. The test fixture uses an OpenLDI chipset DUT board. The Characterization Software Components (CSC) takes the raw test data and converts it to an easy-to-understand visual format.

The data generator/analyzer uses ports to identify groups of generator and analyzer signals. In the OpenLDI deserializer test example, there are two generator ports and two analyzer ports. The generator ports, Port 1 and Port 3, supply the two frequencies required for testing the LVDS deserializer. The analyzer ports, Port 2 and Port 4, sample the data.

For the first set of tests, the data generator/analyzer creates the high-frequency serial data at 333 MHz, which corresponds to 333-Mb/s NRZ data generation. The generator also provides the serializer's input clock at 1/7 the serial data rate. The serializer then generates the LVDS clock input to the deserializer. The analyzer monitors the clock out from the deserializer and samples the data off of the seven parallel data terminals.

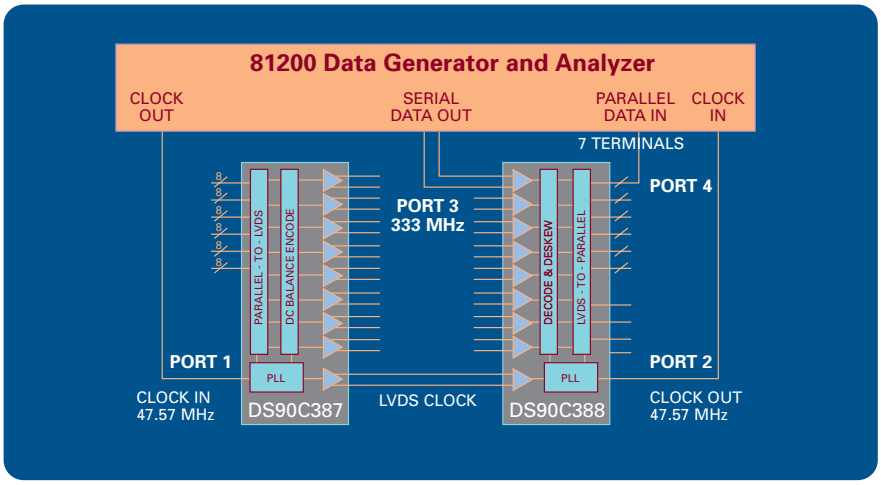


Figure 3. The test setup for the OpenLDI DUT interface board

The first analysis that uses the visual display capability of the CSC shows the actual recoverable bit width of the serial data. Sweeping the serial data delay and checking the BER at the parallel Port 4 allow the data bit width to be displayed.

Figure 4 shows the delay vs. BER for the first two of the seven parallel bits. The bit width at 333 Mb/s is nominally 3 ns, but as the BER graph shows, the recovered bit is about 2.4 ns wide. On each side of the valid-data window, the BER increases to a nonzero value. The BER is a constant value for each of the serial bits preceding and following the bit being checked for correctness. The values are constant but not at 1 because of the repetitive bit pattern used in this test. If the bit pattern had instead been a PRBS pattern, then the BER for each of the other bits would be 0.5, which means there is an equal, and random, chance that the bit would be either 1 or 0.

BER Eye Diagram

The next analysis tool is the BER Eye Diagram. The CSC generates this diagram by sweeping the sampling delay and the threshold of the analyzer on Port 4. The graph displays the BER as a color at each sampling point. The result is an eye pattern with the black center representing the correctly sampled data. Other colors show the increasing errors as the sample point moves further away from the window **(Figure 5)**.

This eye pattern differs from an oscilloscope eye diagram because it does not simultaneously show multiple transitions. An oscilloscope eye diagram displays signal-integrity information such as overshoot, undershoot, and edge jitter. A BER eye diagram demonstrates the valid-data window for the recovered bits, which ultimately depends on receiver sampling performance in addition to signal integrity.

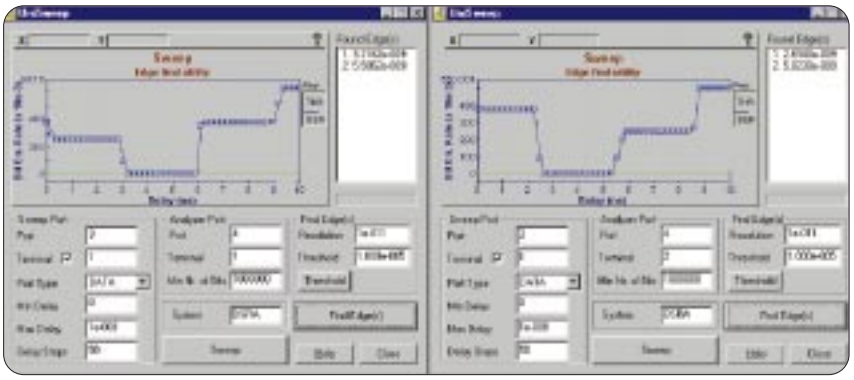


Figure 4. The delay vs. the BER for the first two of seven parallel bits shows the recoverable bit is about 2.4 ns wide.

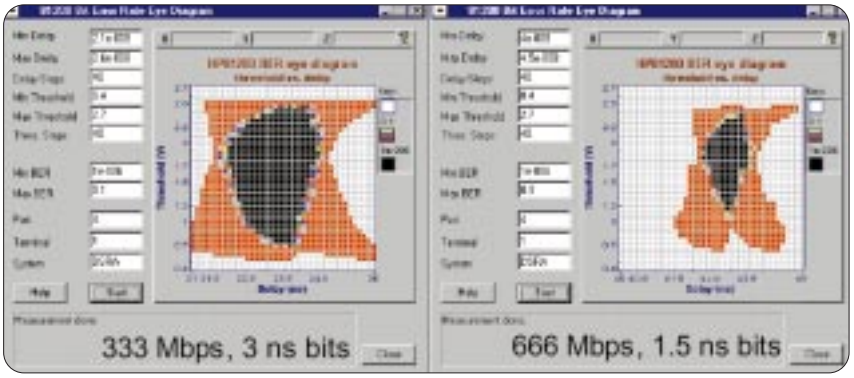


Figure 5. BER eye diagrams for two data rates show how the bit width decreases as the signaling frequency increases.

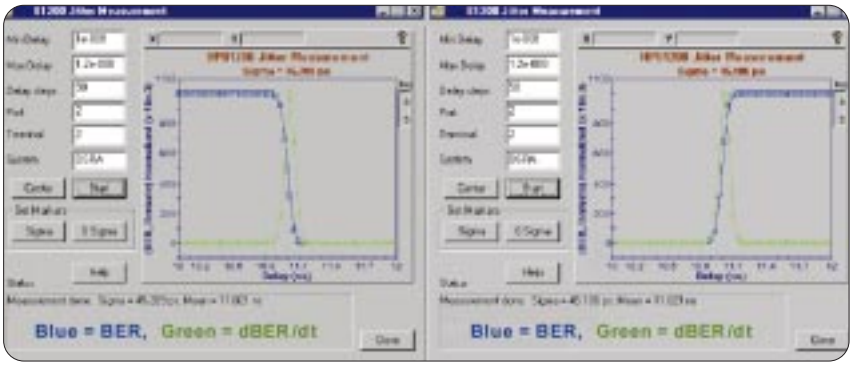


Figure 6. The deserializer's recovered clock-out jitter shows symmetrical jitter when using the same threshold (1.4 V).

Figure 5 visually emphasizes the useable portion of the serial bit width that was also shown in **Figure 4**. The BER eye width for Port 4, terminal 1, at 333 Mb/s shows the same 2.4-ns bit width as in the serial-port delay vs. BER graph.

The BER eye diagram for the 666-Mb/s serial data shows how the bit width decreases as the signaling frequency increases. The graph on the right shows that although the nominal bit width at 666 Mb/s is 1.5 ns, the valid-data window delivered by the receiver and deserializer is really about 1.1 ns wide.

This BER eye diagram is useful in characterizing receiver performance. It allows examining the eye diagram for each individual bit. At the highest performance level, these eye diagrams must show limited variation between bits to ensure there is maximum margin for board and cable skew. This characterization helps system designers to achieve reliable data transfers.

Recovered Clock Jitter

The deserializer's recovered clock-out jitter can also be examined with the CSC. In this case, the data generator/analyzer creates a histogram using the BER measurement. It performs these histogram measurements on a running device to obtain accurate jitter measurements. The CSC uses the deviation of the BER (dBER/dt) to calculate the jitter. It measures the signal transitions by selectively looking at the pass-to-fail and the fail-to-pass BER transitions.

Figure 6 shows the jitter on both the rising edge and the falling edge for the deserializer recovered clock-out signal. Because the sampling point for the analyzer is set at the same point for both the high and low transitions (1.4 V in this case), the jitter is symmetrical on the transitions. Setting the sampling point at different thresholds for the rising transition (2 V) and falling transition (0.8 V) results in different mean transition times for each of the edges.

The CSC also provides calculations for sigma and 6-sigma analysis of the histogram. The Sigma button displays a measurement that corresponds to the RMS jitter, while the 6-Sigma button displays a measurement that corresponds to a peak-to-peak jitter measurement. In **Figure 6,** the CSC reports that RMS jitter is about 45.2 ps for both the rising and falling edges of the deserializer clock-out.

Some applications are suitable for more than one of the various LVDS technologies, but there are others in which only one would excel. Plain old standard LVDS excels in applications requiring driving relatively short interconnects, and also where EMI is a critically sensitive issue for the interconnect, such as in display technology.

Bus LVDS excels at driving heavily loaded backplanes such as those used in telecommunications systems. It also works well in distributing signals from a single driver to multiple receivers. BLVDS also finds applications in driving bussed cable interconnects of a few meters in length.

GLVDS could work in very low-power applications such as remote base stations where power may be locally supplied and generated by wind or sun. It could also be useful as a chip-to-chip interconnect for very short distances. The main function for GLVDS might be as the interconnect technology for chips that have power supplies of 1 V or less. Low-Voltage Differential Signaling will continue to evolve toward more and more system applications.

81200 Provides the Tools to Test LVDS

Testing and evaluating LVDS-based components and systems is a challenge. Not only are the data rates very high and the signals differential, but the types of tests required are often complex and time consuming to perform. The Agilent 81200 provides an easier way to evaluate a design or perform manufacturing tests. It provides a number of visual presentations that allow you to quickly analyze measured data and evaluate the outcome of tests.

The Agilent 81200 data generator/analyzer platform is a flexible real-time stimulus and response system that now works at up to 2.67 Gb/s for up to 64 channels. It provides chip control signals, divided or multiplied clock signals, 1-Mb/s to 2.67-Gb/s operation with proprietary formats, as well as LVDS load generation or analysis.

Powerful sequencing capabilities and full control of pulse parameters for each individual channel mean that you can really stress your device under test (DUT). The system generates pseudo random word sequences (PRWS) and pseudo random binary signals (PRBS) up to 215-1. Analysis is in real time, saving you time because no post-processing is necessary.

If you work on telecommunications multiplexers and demultiplexers (mux/demux), SERDES (serializer/deserializer), or transmitters and receivers, you can take advantage of the thorough parallel BER measurements of the ParBERT 81250 system. For compliance testing, it generates PRWS and PRBS up to 231-1, and also has sophisticated synchronization features.

For more information, check 5 on the reply card.